AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to Fig. 1 on Sheet 1.

Attachment: Replacement sheet

REMARKS

We wish to bring to the examiner's attention three other cases currently pending in the U.S. Patent Office that are closely related to the present application. They are as follows:

Application No.: 10/280,492
Applicants: Lawrence C. West et al.
Filed: October 25, 2002
Title: OPTICAL READY WAFERS
Art Unit: 2883
Examiner: Brian Healy

Application No.: 10/280,505
Applicants: Claes Bjorkman et al.
Filed: October 25, 2002
Title: OPTICAL READY SUBSTRATES
Art Unit: 2874
Examiner: Sarah U. Song

Application No.: 10/623,666
Applicants: Claes Bjorkman et al.
Filed: July 21, 2003
Title: OPTICAL READY SUBSTRATES
Art Unit: 2874
Examiner: S. U. Song

We have amended the claims to address the examiner's §112 concerns. We also added new dependent claims 55 and 56. After entering the amendments, claims 32, 34, 35, and 48-56 will be pending in this application.

The examiner objected to Fig. 1 because S_2O_2 should be SiO_2. We have amended Fig. 1 to correct that error. The corrected drawing is attached hereto.

The examiner rejected claim 48 under 35 U.S.C. §112, 2nd paragraph because supposedly "it is unclear how 'a first semiconductor material' can simultaneously be part of the carrier substrate while also being formed 'above the front side of the carrier substrate'." We note, however, that the claim does not recite that the first semiconductor layer, which has an upper surface that defines the top surface, is made of the first semiconductor material. Moreover, it is

not inconsistent that both the substrate and the first layer comprise a first semiconductor material (e.g. Si), though claim 48 does not recite that.

We have amended claim 32 to make it less wordy by simply stating upfront that the substrate is made at least in part of silicon. This is merely stating upfront a limitation that appeared later in the same claim.

The examiner rejected claims 32, 34, 35, 48-53 under 35 U.S.C. §103(a) as being unpatentable over U.S. 5,987,196 (Noble) in view of U.S. Patent Application 2002/0146865 A1 (Hoel) and U.S. 5,098,861 (Blackstone). The examiner admits that "Noble does not indicate that the optical-ready substrate is sent to a purchaser that will subsequently fabricate microelectronic circuitry thereon by using a second set of semiconductor processes." To supply that which is missing from Noble, the examiner relies on the other two references about which he has the following to say:

> Hoel teaches the benefits of turn around time and cost reduction by semi-customizing integrated circuit fabrication wherein a first set of commonly used, or shared, fabrication processes re used to partially fabricate standard portions of integrated circuits shared among many final integrated circuit designs which are stored in inventory and are available for later customization using a second set of fabrication processes.
>
> It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the first set of fabrication processes of Noble forming optical signal circuitry and to use the second set of fabrication processes to customize the device, in order to reduce the turn around time and reduce costs, as taught by Hoel.
>
> Blackstone teaches that it is known to partially fabricate a semiconductor wafer and then sell the partially fabricated wafer to a "'convention' semiconductor manufacturer who will complete the semiconductor fabrication process utilizing traditional planar semiconductor fabrication techniques."

With regard to Hoel, we note that contrary to what the examiner seems to believe it has no applicability to Noble, at least not in the manner proposed by the examiner. Hoel involves semiconductor circuits for which both standardized masks and customized masks are used in combination to produce final circuits. The standardized masks are used in fabricating all of the circuits and the customized masks are used to complete the fabrication process to produce particular designs. In other words, one set of customized masks in combination with the

standardized masks will produce one circuit design and a second set of customized masks in combination with the standardized masks will produce a second circuit design. Thus, the circuit can be fabricated up to the point at which the customized masks are to be used and then inventoried for later use. When the specific design for the final circuit is decided upon, then the inventoried product can be used to complete the fabrication process. In that way, it is not necessary to start the fabrication process from the very being once each new design is developed, so long as that new design is based upon the standard design.

The masks for which Hoel uses this approach are the masks for fabricating the vias and the metal interconnects. That is, Hoel's technique assumes that the underlying arrangement of circuit devices is the same for the different possible customized circuit designs. The only thing that changes is the way those underlying circuit devices are interconnected. There is nothing in Noble that suggests the circuits that are being fabricated are of the type that would benefit from such an approach.

But even if Noble did employ circuits that would benefit from the technique disclosed by Hoel, the use of Hoel's technique in fabricating Noble's circuits would not result in the claimed invention. Rather, applying Hoel to Noble would modify the fabrication process in a way that only affects how the underlying electrical devices are interconnected. It would not result in a process in which the optical circuitry is fabricated in a first phase after which the substrates are put into inventory for use at a later time to fabricate the overlying electrical circuitry.

Hoel does not teach nor does he in any way suggest dividing the fabrication process into two phases the first of which is used to fabricate one set of circuits (e.g. optical circuits) and the second of which is used to fabricate a second set of circuits (e.g. microelectronic circuitry). Indeed, Hoel does not in any way suggest using his technique on those portions of the fabrication process that precede the phases during which vias and metal interconnects are fabricated. In addition, neither Hoel, nor any of the other references relied on by the examiner, teaches or suggests that underlying optical circuitry that is fabricated in Noble could be standardized arrangements that could be later used to support different customized arrangements

of microelectronic circuitry that are to be subsequently fabricated in layer 20 of the Noble structure.

In short, there is no motivation to combine Hoel with Noble in the manner proposed by the examiner. But if a person of ordinary skill in the art were to combine Hoel with Noble, the result would not be the claimed invention.

With regard to Blackstone, we note that the "partially fabricated wafers" that Blackstone proposes be sold have no circuits in them. Indeed, they do not even have any devices in them. They are simply substrates in which two buried layers have been formed beneath an upper layer of silicon, namely, a silicide layer on top of a SiO_2 or SiN layer. The silicide layer provides a fast diffusion path for later diffusion of N+ or P+ dopants into the wafers to form high conductivity buried layers that have uniform thickness. Backstone teaches nothing more that providing substrates that have been modified to accommodate the later fabrication of complimentary semiconductor structures. According to Blackstone:

> The metal silicide layer disposed internally to the bonded semiconductor substrate enables conventional semiconductor planar fabrication technology to form a buried layer in the first semiconductor wafer which is shallow, and of uniform thickness. (Col. 3, lines 13-17).

Blackstone's process is very similar to what is done in fabricating an SOI wafer in which the upper silicon layer is provided for later fabricating microelectronic circuitry and a buried thin layer of insulating material, e.g. SiO_2, is provided to isolate the upper silicon layer from the rest of the silicon substrate. Clearly, the idea behind Blackstone is to provide the semiconductor fabricator with a substrate that does not constrain the fabricator with regard to the layout of the circuits that can be fabricated into the substrates.

Blackstone neither teaches nor suggests fabricating some circuitry in a buried layer before providing the substrate to another entity which then fabricates further circuitry in an overlying layer. Indeed, Blackstone teaches away from customizing the preliminary fabrication process in any way that results in a substrate that is not "generic." Blackstone makes this clear in his discussion of the drawbacks of the prior art approaches:

> One drawback of this technique is that wafer 70, FIG. 3A, becomes "customized" immediately upon the first doping and diffusion steps 72-74 shown in FIG. 3A. Accordingly, the prior art lacks a method for processing one or more semiconductor wafers to provide a semiconductor substrate that is "generic" or partially processed utilizing more sophisticated semiconductor processing techniques, while allowing the partially processed substrate to be subsequently further processed and finished utilizing conventional semiconductor planar processing techniques, thus insuring that the substrate will provide matched semiconductor elements or devices of equal thickness. (Col. 2, lines 50-62).

Thus, a person of ordinary skill in the art would not be motivated to employ the techniques of Blackstone in the manner proposed by the examiner. The examiner's proposed modification of Nobel's fabrication process would yield partially-completed structures that could not even remotely be characterized as generic, which is a result that is contrary to the teachings of Blackstone.

However, even if one were motivated to employ Blackstone's techniques in the fabrication of Noble's structures, the result would be a substrate that has been modified in some way that is useful to subsequent processing of the circuitry (optical and electrical) that is to be later fabricated into that substrate. That is not the claimed invention.

For the reasons stated above, we submit that the claims are in conditions for allowance and ask the examiner to allow them.

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Respectfully submitted,

By _____

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Attachments